AMENDMENTS TO THE CLAIMS

The following claims are given merely for ease of reference. ***No amendments are introduced.***

1. (Previously presented) A system, comprising:

(A) a material metering machine having a load cell, the load cell being configured to generate an analog signal, the analog signal being indicative of a load on the load cell;

(B) an analog-to-digital converter configured to convert the analog signal into a digital signal, the digital signal having a sampling rate of 307.2 kHz;

(C) a preliminary decimation element comprising:

(C1) a first finite-impulse-response (FIR) filter having a decimation ratio of 16, the first FIR filter being configured to reduce the sampling rate of the digital signal from 307.2 kHz to 19.2 kHz; and

(C2) a second FIR filter serially coupled to the first FIR filter, the second FIR filter having a decimation ratio of 16, the second FIR filter being configured to reduce the sampling rate of the digital signal from 19.2 kHz to 1200 Hz;

(D) a primary decimation element serially coupled to the preliminary decimation element, the primary decimation element comprising:

(D1) a third FIR filter having a decimation ratio of 2, the third FIR filter being configured to reduce the sampling rate of the digital signal from 1200 Hz to 600 Hz;

(D2) a fourth FIR filter having a decimation ratio of 10, the fourth FIR filter being configured to reduce the sampling rate of the digital signal from 600 Hz to 60 Hz; and

(D3) a fifth FIR filter having a decimation ratio of 6, the fifth FIR filter being configured to reduce the sampling rate of the digital signal from 60 Hz to 10 Hz; and

(E) a filter bank serially coupled to the primary decimation element, the filter bank comprising:

(E1) selectable filters, each filter being configured to reduce the noise, the selectable

filters including a filter having a sub-hertz 3-dB cutoff frequency, the selectable filters comprising a filter selected from the group consisting of:

(E1a) a SINC filter; and

(E1b) a raised cosine filter; and

(E2) a selectable filter switch configured to select a selectable filter, the selectable filter being selected as a function of operating criteria, the operating criteria being associated with the material metering machine, the operating criteria being determined through a closed feedback loop.

2. (Previously presented) A system, comprising:

a material metering machine comprising a decimation element, the decimation element configured to reduce an initial sampling rate of a digital signal to a reduced sampling rate; and

a filter bank, the filter bank comprising:

an input node adapted to receive the digital signal from the decimation element, the digital signal having noise from the material metering machine; and

selectable filters, each selectable filter having a sub-hertz 3-dB cutoff frequency, each filter being configured to reduce the noise.

3-18. (Canceled)

19. (Original) A filtering apparatus, comprising:

a primary input node configured to receive a digital signal, the digital signal having an initial sampling rate, the digital signal further having line noise; and

a primary decimation element having a decimation ratio, the primary decimation element further having a filter length, the primary decimation element being configured to reduce the line noise at 50 Hz, the primary decimation element further being configured to reduce the line noise at 60 Hz, the primary decimation element further being configured to reduce the initial sampling rate to a reduced sampling rate as a function of the decimation ratio.

20. (Original) The apparatus of claim 19, wherein the initial sampling rate is 1200 Hz.

21. (Original) The apparatus of claim 19, wherein the reduced sampling rate is 10 Hz.

22. (Original) The apparatus of claim 19, wherein the primary decimation element comprises:

a first filter having a decimation ratio of 2;

a second filter serially coupled to the first filter, the second filter having a decimation ratio of 10; and

a third filter serially coupled to the second filter, the third filter having a decimation ratio of 6.

23. (Original) The apparatus of claim 19, further comprising an analog-to-digital (A/D) converter, the A/D converter being configured to receive an analog signal, the A/D converter further being configured to convert the analog signal into the digital signal, the A/D converter further being configured to provide the digital signal to the primary input node.

24. (Original) The apparatus of claim 19, further comprising a preliminary decimation element having an input, the preliminary decimation element further having an output, the output of the preliminary decimation element being communicatively coupled to the primary input node, the preliminary decimation element comprising:

a first filter having a decimation ratio of 16; and

a second filter serially coupled to the first filter, the second filter having a decimation ratio of 16.

25. (Original) The apparatus of claim 24, further comprising an analog-to-digital (A/D) converter, the A/D converter being configured to receive an analog signal, the A/D converter further being configured to digitize the analog signal, the A/D converter further being configured to provide the digitized signal to the input of the preliminary decimation element.

26. (Original) A filtering method, comprising the steps of:

receiving a digital signal, the digital signal having an initial sampling rate, the digital signal further having line noise;

filtering the line noise at 50 Hz;

filtering the line noise at 60 Hz; and

reducing the initial sampling rate of the digital signal to a reduced sampling rate.

27. (Original) The method of claim 26, wherein the step of receiving the digital signal comprises the step of receiving a digital signal having a sampling rate of 1200 Hz.

28. (Original) The method of claim 26, wherein the step of filtering the line noise at 50 Hz comprises the step of cascading the digital signal through multiple filters.

29. (Original) The method of claim 26, wherein the step of filtering the line noise at 60 Hz comprises the step of cascading the digital signal through multiple filters.

30. (Original) The method of claim 26, wherein the step of reducing the initial sampling rate comprises the step of cascading the digital signal through multiple filters.

31. (Original) The method of claim 26, further comprising the step of cascading the digital signal through multiple filters.

32. (Original) The method of claim 31, wherein the step of cascading the digital signal through multiple filters comprises the step of directing the digital signal through a filter having a decimation ratio of 16.

33. (Original) The method of claim 31, wherein the step of cascading the digital signal through multiple filters comprises the step of directing the digital signal through a filter having a decimation ratio of 2.

34. (Original) The method of claim 31, wherein the step of cascading the digital signal through multiple filters comprises the step of directing the digital signal through a filter having a decimation ratio of 10.

35. (Original) The method of claim 31, wherein the step of cascading the digital signal through multiple filters comprises the step of directing the digital signal through a filter having a decimation ratio of 6.

36. (Original) The method of claim 26, further comprising the steps of:

receiving an analog data signal from a load cell, the load cell being located on a material metering machine; and

converting the analog signal into the digital signal.

37. (Original) The method of claim 26, wherein the step of converting the analog signal comprises the step of:

generating a digital signal having a sampling rate of 1200 Hz.

38. (Previously presented) The system of claim 1, wherein the preliminary decimation element, the primary decimation element, and the filter bank are located within a single digital signal processor.

39. (Previously presented) The system of claim 2, wherein the decimation element and the filter bank are located within a single digital signal processor.

40. (Previously presented) The apparatus of claim 19, wherein the primary input node and the primary decimation element are located within a single digital signal processor.